REMARKS

Present Status of the Application

The Office Action rejected all pending claims 1-20. Specifically, the Office Action rejected claims 1-4 and 6-13 under 35 U.S.C. 102(e) as being anticipated by Sato (U. S. publication 2002/0140645). The Office Action also rejected claims 5 and 14-20 under 35 U.S.C. 103(a) as being unpatentable over Sato. Applicant has amended claims 1, 12 and 16 to improve clarity. Applicant has also amended specification to correct typographic errors. After entry of amendments, claims 1-20 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Discussion of Claim Rejections under 35 USC 102

The Office Action rejected claims 1-4 and 6-13 under 35 U.S.C. 102(e) as being anticipated by Sato. Applicant respectfully traverses the rejections for at least the reasons set forth below.

Applicants have amended claims 1 and 12 to more specifically define the second clock in response to the Office action in "*Response to Arguments*".

Now, as for example shown in FIG 6 of the present invention, the clock CLK1 is partitioned into the clocks CLK2A and CLK2B. The second clock is used for a discharged frame by inputting a reset signal.

In this operation mechanism, for example, every period in the first clock has a second clock for temporarily switching the TFT off to reset the threshold voltage level.

To more understand the discharge effect from the second clock, actually, the second clock is not necessary to be the same frequency as that of the first clock. The second clock can be arranged, for example, to be slower in frequency than the first clock, so that the TFT can be temporarily turned off without affecting the view effect. The same frequency for the second clock is in considering due to human eye's function, so that even if the second clock causes the black image, the human eye does not sense it.

In re Sato, the clock CLK+ and clock CLK–, as referred by the Office Action, are pixel clock signals ([0088], line5-7). One is for p-type switching transistor and one is for n-type switching transistor ([0098]), ***so that the clock CLK+ and the clock CLK - have the precise phase shift by 180 degrees, corresponding to the n-type and p-type transistors.*** In other words, the clock CLK+ should be exactly inverse from the clock CLK-.

In the present invention, the second clock is not necessary to be exactly inverse from the first clock as for example, shown in FIG. 6. Particularly, in Fig. 4 of Sato, the DATA are input between the start pulse ST and the low level reset signal R ([0093], linc 4). Clearly, the clocks CLK+ and CLK– of Sato are not provided to perform the function as recited in the present invention. Sato failed to disclose the operation feature of the claimed invention.

It is respectfully reminded that the hindsight and the improper construing Sato should be carefully avoided.

With at least the same foregoing reasons applied to independent claims 1 and 12, dependent claims 1-4, 6-11 and 13 are distinguish over Sato as well.

Discussion of Claim Rejections under 35 USC 103

The Office Action also rejected claims 5 and 14-20 under 35 U.S.C. 103(a) as being unpatentable over Sato. Applicant respectfully traverses the rejections for at least the reasons set forth below.

With at the same the foregoing reasons, Sato failed to disclose features of dependent claims 5 and 14-15.

With respect to independent claim 16, in addition to the same foregoing reasons applied to claims 1 and 12, the clock CLK+ and CLK- are not the first clock CLK2A and the second clock CLK2B. Also and, one of the clocks CLK2A and CLK2B is used as the rest clock to reset the pixel unit for each frame. In Fig. 4 of Sato, the reset signal R is not one of the clocks CLK+ or CLK- of Sato.

In the present invention, the first clock and the second clock of the present invention are alternatively activated in every one clock period.

In conclusions, the present invention uses the reset signal to reset the pixel unit, particularly to temporarily in time to switch the driving transistor 102 off ***in every signal input period.*** *In the conventional skill, the driving transistor 102 is always on to keep the LED 104 to be*

continuous on. In the present invention, the second clock has a fixed delay time to the first clock and is used for the discharge frame to temporarily switch the driving transistor off. Sato fails to disclose this arrangement of the second clock in the claimed invention. Clocks CLK + and CLK – of Sato are for n-type and p-type transistors ([0088], [0098]), ***and are not the first clock and the second clock of the present invention.***

For at least the foregoing reasons, Applicant respectfully submits that independent claims 1, 12, and 16 patently define over the prior art references, and should be allowed. For at least the same reasons, dependent claims 2-11, 13-15, and 17-20 patently define over the prior art references as well.

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CONCLUSION

For at least the foregoing reasons, it is believed that all the pending claims 1-20 of the invention patently define over the prior art and are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

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